American Journal of Modern Physics
2018; 7(4): 166-172
http://www.sciencepublishinggroup.com/j/ajmp
doi: 10.11648/j.ajmp.20180704.14
ISSN: 2326-8867 (Print); ISSN: 2326-8891 (Online)

Modeling and Characterization of Inconsistent Behavior of Gate Leakage Current with Threshold Voltage for Nano MOSFETs

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To cite this article:
Yashu Swami, Sanjeev Rai. Modeling and Characterization of Inconsistent Behavior of Gate Leakage Current with Threshold Voltage for Nano MOSFETs. *American Journal of Modern Physics*. Vol. 7, No. 4, 2018, pp. 166-172. doi: 10.11648/j.ajmp.20180704.14

Received: July 13, 2018; **Accepted**: August 19, 2018; **Published**: September 15, 2018

Abstract: A strange relationship of gate leakage current and threshold voltage variation for nano MOSFETs is analyzed using factual strategy and subsequently a physical model is proffered. The gate leakage current increments with the threshold voltage before it diminishes at higher threshold voltage in nanoscale devices. This inconsistent behavior of gate leakage current with threshold voltage variations is precisely clarified in the manuscript through the concept of accord between two contrary operations: threshold voltage roll-off impact and gate leakage current reliance on surface potential. The tunneling gate leakage current density diminishes with threshold voltage over surface potential. However, the threshold voltage roll-off impact causes higher threshold voltage for larger channel length devices. The net gate leakage current is adjusted by these two contrary functions of threshold voltage. In addition, the rate of accretion of the gate leakage current with threshold voltage variation is also analyzed. The impact of the increase in the power supply voltage on the rate of accretion of the gate leakage current vs. threshold voltage curve is also explored. Thorough methodical TCAD simulations are accomplished to validate the proffered models. Both the experimental outcomes, TCAD simulations and physics based models are implemented to uncover and clarify the threshold voltage gate leakage relationship, particularly for nano MOSFETs. The proposed notion is not currently captured in conventional gate leakage nano device models, hence the proffered physical models may be utilized in progression of reliable and trustworthy TCAD simulation tools for nano devices.

Keywords: Gate Leakage Current, Line-Edge Roughness, Nano MOSFET, Oxide Thickness Variation, Random Dopant Fluctuation, Threshold Voltage Roll-off Impact

1. Introduction

The device characteristic variations have developed as a noteworthy barrier for CMOS technology scaling [1-3]. Of specific significance is the factual variation of threshold voltage (V_{TH}) and gate leakage current (I_{GL}) which confines the power and performance measurements. It also prompts to critical output restrictions for both analog, digital and computerized memory/SRAM design [4-6]. A physical comprehension of the threshold voltage and gate leakage current (V_{TH})-(I_{GL}) relationship is critical for both device modeling and circuit design especially at nanoscale technology [7-10]. It has been noted that the (V_{TH})-(I_{GL}) relationship to a great extent has been overlooked and ignored for long channel devices, profoundly scaled 45nm and past technologies. However, the (V_{TH})-(I_{GL}) relationship cannot be ignored for nano devices, particularly for below 45nm scaled technologies. In this manuscript, we present a comprehensive study on characterizing the inconsistent behavior of gate leakage current with threshold voltage variation particularly for nano MOSFETs. The inconsistent (V_{TH})-(I_{GL}) relationship is accurately modeled after analyzing the experimental measurements and factual investigation performed on more than 20,000 MOSFETs fabricated with advanced 45nm *PD-SOI* technology. We evidently demonstrate that the inconsistent behavior of gate leakage current with threshold voltage variation emerges exceptionally for nanoscaled MOSFETs. Both the experimental outcomes and physics

based models are acquainted to uncover and clarify the (V_{TH})-(I_{GL}) relationship particularly for nano MOSFETs.

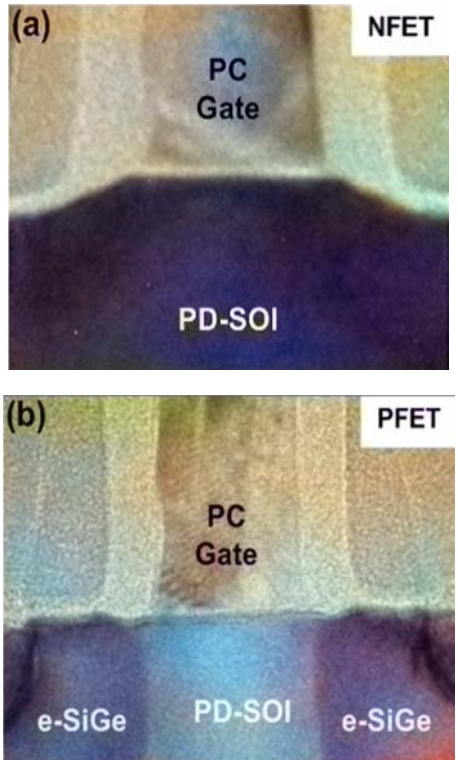


Figure 1. *TEM image of a PD-SOI (a) N-MOSFET and (b) P-MOSFET device used to examine and model inconsistent (V_{TH})-(I_{GL}) relationship.*

2. Model Device Fabrication Approach

For the comprehensive study on characterizing the inconsistent behavior of gate leakage current with threshold voltage variation, *PD-SOI* MOSFETs are fabricated utilizing 45nm technology. Figure. 1 represents the typical cross-section TEM image of a N-MOSFET and P-MOSFET device used to examine and model inconsistent (V_{TH})-(I_{GL}) relationship using four discrete threshold voltage device designs (V_{TH1}-V_{TH4}) [7]. The device development highlights the fabrication process with the following features: numerical aperture value of 1.2, 193nm immersion lithography designing, enhanced Dual-Stress Liner (DSL), Stress Memorization Technique (SMT), Advanced Annealing (AA), and close-proximity embedded advanced e-SiGe [11-12]. The model MOSFETs with Poly-Si/SiON gate stack are fabricated for four discrete threshold voltages (V_{TH1} - V_{TH4}) with their nominal threshold voltage characteristics as $V_{TH1}<V_{TH2}<V_{TH3}<V_{TH4}$. The threshold voltage variance features are acknowledged through the substrate and halo doping practice. The device dimension measurements are assessed by adjusting the physical estimations in TEM and XPS. N-MOSFET contains 10 fingers with a width (W_F) of 400nm and normal gate length (L_G) of 40nm for each finger. Threshold voltage is characterized by Constant Current Threshold Voltage Extraction Technique (CCM) [13-14] and estimated at $V_{DS}=V_{DD}$ for V_{TSAT} and $V_{DS}=50mV$ for V_{TLIN}. The V_{TSAT} and V_{TLIN} represent the respective threshold voltages of the device while operating in saturation and linear region. Gate leakage current (I_{GL}) is estimated under inversion condition where $V_{GS}=V_{DD}$. The V_{DD} is biased at 0.9V.

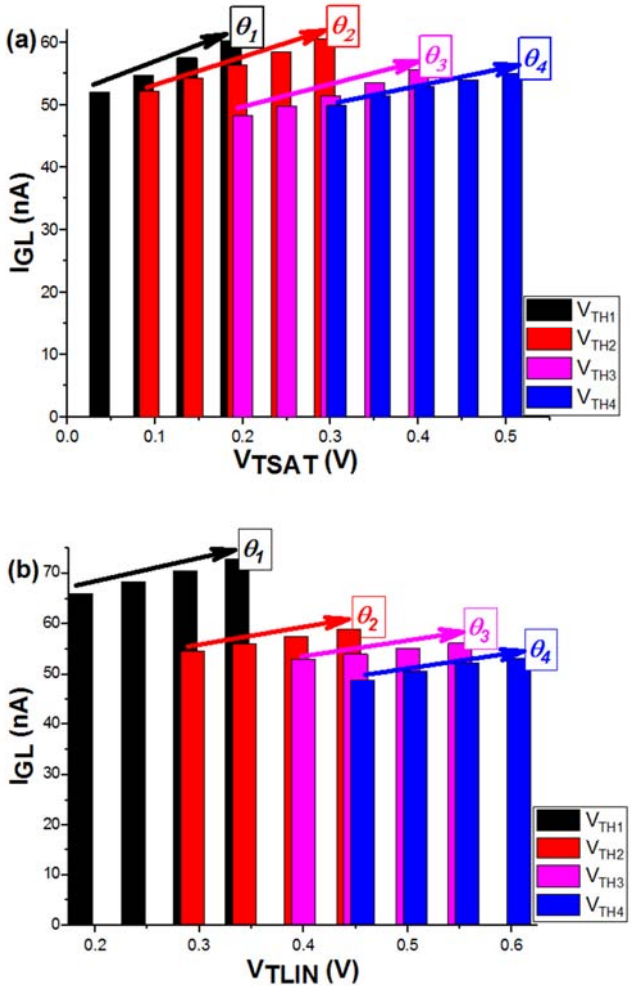


Figure 2. *Gate leakage current extracted under inversion condition as for (a) V_{TSAT} and (b) V_{TLIN} for N-MOSFETs with discrete limit voltages (V_{TH1}-V_{TH4}). For V_{TH1} to V_{TH4} device lot, the rate of increment of gate leakage current with the threshold voltage variations is accordingly represented by Θ_1 to Θ_4. The contour plots are density ellipsoids as extracted from the bivariate normal distribution fit to the X and Y factors with the likelihood of 0.9. Same conditions apply to the other plots in this manuscript.*

3. Simulation Analysis and Model Formalism

Figure. 2 illustrates the typical threshold voltage and gate leakage current (V_{TH})-(I_{GL}) relation. The compiled data is plotted after performing simulation and extraction process on over 20,000 N-MOSFET devices from discrete lots and wafers. For V_{TH1} to V_{TH4} device lot, I_{GL} monotonically increments with the threshold voltage inside every particular plan for V_{TH1} to V_{TH4}; however, the accretion rate of gate leakage current diminishes with the increase in nominal threshold voltage. The characteristics are observed in both the operating regions (saturation and linear region) of the nano

device. The rate of accretion of gate leakage current with the threshold voltage variations for discrete design lot (V_{TH1} *to* V_{TH4}) is respectively represented by Θ_1 to Θ_4. For precise and specific representation, Table I exhibit the simulation results in tabular format. Table I justifies the logic when the extraction is restricted to devices of same design lot. This inconsistent behavior is visualized exceptionally for nanoscaled MOSFETs but missing in long channel devices.

Table 1. *Rate of Accretion of Gate Leakage Current vs. Threshold Voltage.*

Parameter	V_{TSAT} (V_{DS}=0.9V)	V_{TLIN} (V_{DS}=0.05V)
Θ_1	5.49e-8	5.47e-7
Θ_2	4.19e-8	3.06e-7
Θ_3	3.21e-8	1.54e-7
Θ_4	3.07e-8	1.49e-7

A prior model on relation between threshold voltage and gate leakage current reports that the increment in threshold voltage result in augmentation of gate leakage current [10]. The obvious threshold voltage variance to the gate leakage streaming over large gate resistance leads to this conclusion that gate leakage current increments with the threshold voltage [10]. The stated notion at nano level technology node is expressly not followed in this study since the voltage drop over the post-salicide 10-finger gate is immaterial in nano devices:

$$V_{TH} \approx I_{GL} R_s \frac{W_F}{L_G \times 10} \tag{1}$$

Using the model device parameters in (1), we get

$$V_{TH} = 0.1\mu A \times 10\Omega/sq \times \frac{400nm}{40nm \times 10} = 1\mu V$$

where R_s represent the gate sheet resistance, W_F and L_G represents the finger width and nominal gate length respectively.

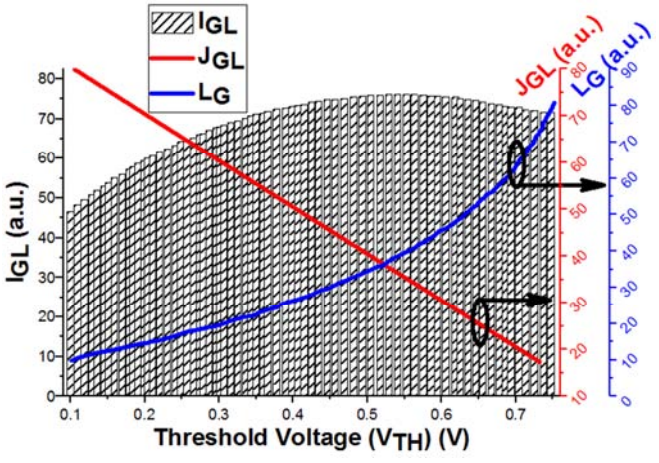


Figure 3. *Typical TCAD standardized simulation results of the correlation of gate leakage current (I_{GL}), gate leakage current density (J_{GL}), channel length (L_G) with threshold voltage (V_{TH}) in reference to this model. The figure illustrates the proffered model (4) and (7) for the inconsistent relation between threshold voltage and gate leakage current for nanoscaled MOSFETs.*

Table 2. *Simulation Parameters used in TCAD Extraction of model (4) & (7).*

Parameter	Value
Channel Length (L_G)	40nm
Channel Width (W)	400nm
Oxide Thickness (T_{OX})	1.2nm
Source surface built-in Potential (Ψ_{bi})	0.7V
Subthreshold Swing (SS)	80mV/dec
Power Supply (V_{DD})	0.9V
Drain Bias (V_{DS})	0.05V/0.9V
Gate Bias (V_{GS})	0.9V
Minimum Depletion Width (W_{DM})	20nm
V_{TH} Long-channel Device (V_{TH0})	0.8V
Operating Temperature (T)	300K

To elucidate and clarify the information, a physical model is proffered which also considers the short channel impacts, prominently, threshold voltage roll-off impact as the main cause for the inconsistent (V_{TH})-(I_{GL}) relationship. The physical components for the inconsistent relation between threshold voltage and gate leakage current are viewed as two-fold contrary operations:

1) Tunneling Gate leakage current density (J_{GL})

The surface potential reduces with the technology node as the oxide thickness is scaled. The tunneling gate leakage current density (J_{GL}) diminishes with V_{TH} over surface potential (ψ_s) similarly as shown in BSIM4 model [15]:

$$J_{GL} = AN_{inv}\left(\frac{V_{GS}}{T_{OX}}\right)\exp\left[\left\{\frac{-8\pi T_{OX}\sqrt{2m_{OX}\emptyset_b{}^3}}{3he|V_{OX}|}\right\}\left(1-B^{\frac{3}{2}}\right)\right\}\times \left\{\frac{20B}{\emptyset_b}\left(\frac{|V_{OX}|-\emptyset_b}{\emptyset_{bo}}+1\right)^{\alpha}\right\}] \tag{2}$$

The variables A and B are used for the simplified representation of the complicated gate leakage current density equation. The variables are equated as:

$$A = \frac{e^3}{8\pi h \emptyset_b \varepsilon_{OX}} \; and \; B = \left(1 - \frac{|V_{OX}|}{\emptyset_b}\right)$$

The auxiliary function N_{inv} represents the density of carriers in inversion layer of channel. It can be represented as:

$$N_{inv} \approx \frac{\varepsilon_{OX}}{T_{OX}} \times SS \times ln\left[1 + exp\left(\frac{V_{GS}-V_{TH}(\Psi_S)}{SS}\right)\right] \tag{3}$$

Using (3) in (2), the gate leakage current density can be approximated as:

$$J_{GL} \approx ln\left[1 + exp\left(\frac{V_{GS}-V_{TH}(\Psi_s)}{SS}\right)\right] \times f(\emptyset_b, \varepsilon_{OX}, T_{OX}, m_{OX}, V_{OX}, V_{GS}, T) \tag{4}$$

Here the values of the functions *f, α, β* are dependent barrier height (Φ_b), dielectric constant (ε_{OX}), electron effective mass in the dielectric (m_{OX}), dielectric thickness (T_{OX}), operating temperature (T), gate voltage (V_{GS}), and overdrive voltage across the dielectric (V_{OX}). *SS* is the Subthreshold Swing.

2) Threshold Voltage roll-off impact (V_{TH} roll-off)

The decline in the device threshold with the reduction in gate length is a widely known short channel effect termed as

threshold voltage roll-off impact. Threshold Voltage roll-off impact causes higher V_{TH} for longer channel length (L_G) devices. As elaborated in [16], this impact can be compactly modeled as:

$$\Delta V_{TH} = V_{TH0} - V_{TH}(\Psi_s) \quad (5)$$

$$\Delta V_{TH} = \frac{24T_{OX}}{W_{DM}}\sqrt{\Psi_{bi}(\Psi_{bi}+V_{DS})} \times \exp(-\frac{\pi L_G/2}{W_{DM}+3T_{OX}}) \quad (6)$$

From (5) and (6), the gate length and the threshold voltage relation can be presented as:

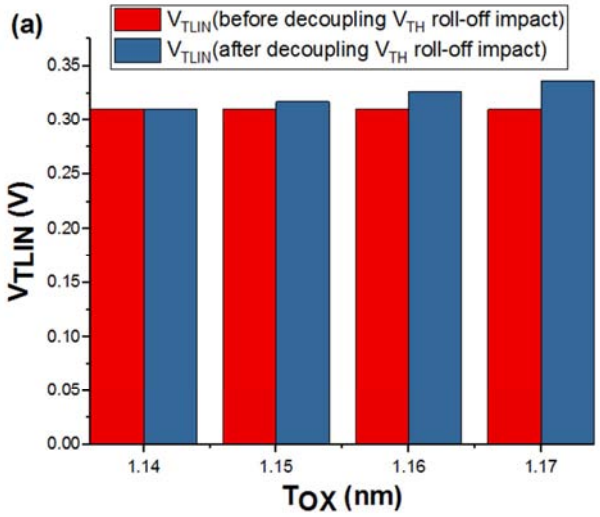
$$L_G = \frac{1}{\eta} \times \ln[\frac{\gamma}{V_{TH0}-V_{TH}(\Psi_S)}] \quad (7)$$

Here the values of η, γ variables are dependent on T_{OX}, V_{DS}, the minimum depletion width W_{DM}, and the source-substrate built-in potential ψ_{bi}. V_{TH0} is the long-channel device threshold voltage.

The net gate leakage current can be represented as:

$$I_{GL} = J_{GL} \times L_G \times W \quad (8)$$

Figure. 3 illustrates the proffered model (4) and (7) for the inconsistent relation between threshold voltage and gate leakage current for nanoscaled MOSFETs. The gate leakage current (I_{GL}) is adjusted between the previously mentioned two contrary functions of V_{TH}. For a particular device design lot, the incline of I_{GL} versus V_{TH} variance relies on the initial V_{TH} position. The slope may alter from positive to negative as elucidated through plotted TCAD simulation results. The simulation parameters used in the TCAD extraction of model (4) and (7) are listed in Table II. Figure. 3 evidently demonstrates typical standardized simulation results of the correlation of gate leakage (I_{GL}), gate leakage current density (J_{GL}), channel length (L_G) with threshold voltage (V_{TH}) in reference to the model (4) and (7).



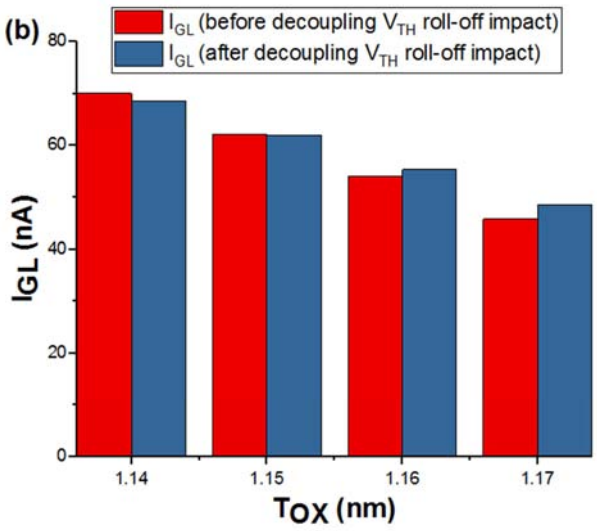


Figure 4. *Demonstration of the relationship of V_{TLIN} and I_{GL} with T_{OX} variance when separating the V_{THI} device design lot by estimated L_G = 40nm, showing that LER prompted threshold voltage roll-off impact overwhelms over the OTV impact. (a) V_{TLIN} variance outwardly shows no association with oxide thickness (T_{OX}) when line-edge roughness (LER) induced threshold voltage roll-off variation is considered. However, the V_{TLIN} variance shows positive association to the oxide thickness (T_{OX}). (b) The gate leakage current (I_{GL}) shows steady negative relation to oxide thickness (T_{OX}) before and after decoupling threshold voltage roll-off impact.*

4. Proffered Model Validation

For the proffered model validation of (4) and (7), we test the essential factors that influence the intrinsic device inconstancy regarding the (V_{TH})-(I_{GL}) relationship by experimentally decoupling the impacts of Random Dopant Fluctuation (RDF), Line-Edge Roughness (LER), and atomic-scale Oxide Thickness Variation (OTV) [1]. For the devices with the size of 400nm×10×40nm, a moderately little RDF-initiated $\sigma V_{TH} \approx 2.5mV$ is assessed in view of the TCAD simulation [4]. To assess LER and OTV independently, we channel the experimental results considering the gate length and oxide thickness. Figure. 4 demonstrates the relationship of V_{TLIN} and T_{OX} variance when separating the V_{THI} device design lot by estimated L_G=40nm, displaying that LER prompted threshold voltage roll-off impact overwhelms over the OTV impact. Figure. 4(a) demonstrates the V_{TLIN} variance shows outwardly no association with oxide thickness (T_{OX}). when line-edge roughness (LER) induced threshold voltage roll-off variation is considered. However, the V_{TLIN} variance shows positive association to the oxide thickness (T_{OX}). Figure. 4(b) presents the fact that the gate leakage current (I_{GL}) shows steady negative relation to oxide thickness (T_{OX}). Hence, we can conclude that the critically observed I_{GL} versus V_{TLIN} uncertainty cannot be primarily credited to the oxide thickness (T_{OX}) variance.

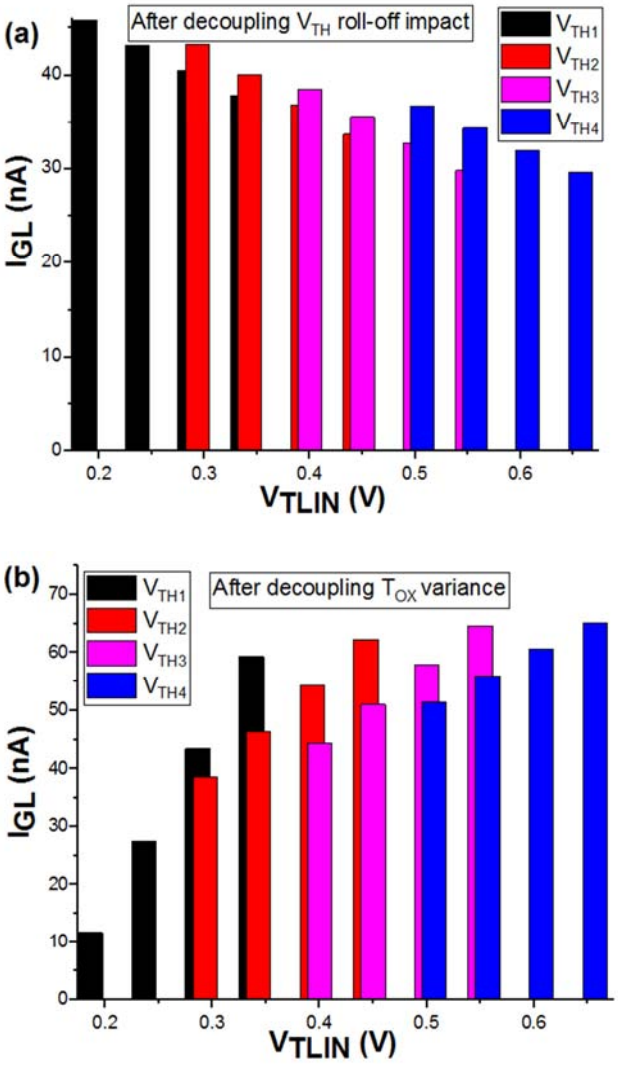


Figure 5. *Gate leakage current versus V_{TLIN} variance (a) after decoupling LER prompted threshold voltage roll-off impact by categorizing the device design lot ($V_{TH1} – V_{TH4}$) with same channel length characteristics of L_g = 40nm and (b) after decoupling the dielectric thickness variance by categorizing the device design lot ($V_{TH1} – V_{TH4}$) with same dielectric thickness (Tox = 1.16nm) devices.*

Figure. 5(a) demonstrates the correlation of I_{GL} versus V_{TLIN} after decoupling LER-prompted threshold voltage roll-off impact by categorizing the device design lot ($V_{TH1} – V_{TH4}$) with same channel length characteristics of L_G = 40nm. Similarly, Figure. 5(b) demonstrates the correlation of I_{GL} versus V_{TLIN} subsequent to the decoupling the OTV impact categorizing the device design lot ($V_{TH1} – V_{TH4}$) with same dielectric thickness of T_{OX} = 1.16nm. Observing the characteristics of the slope of (I_{GL})-(V_{TLIN}) curve for discrete threshold voltage device design lots plotted in Figure. 5(a) and Figure. 5(b), we perceive unexpected inverse patterns, validating that threshold voltage roll-off impact plays a noteworthy part in the inconsistent threshold voltage dependent relationship between I_{GL} and V_{TLIN} variance especially for nanoscaled devices. The statement also supports the illustrations shown in Figure. 2. The results are also in agreement with the proffered model (4) and (7).

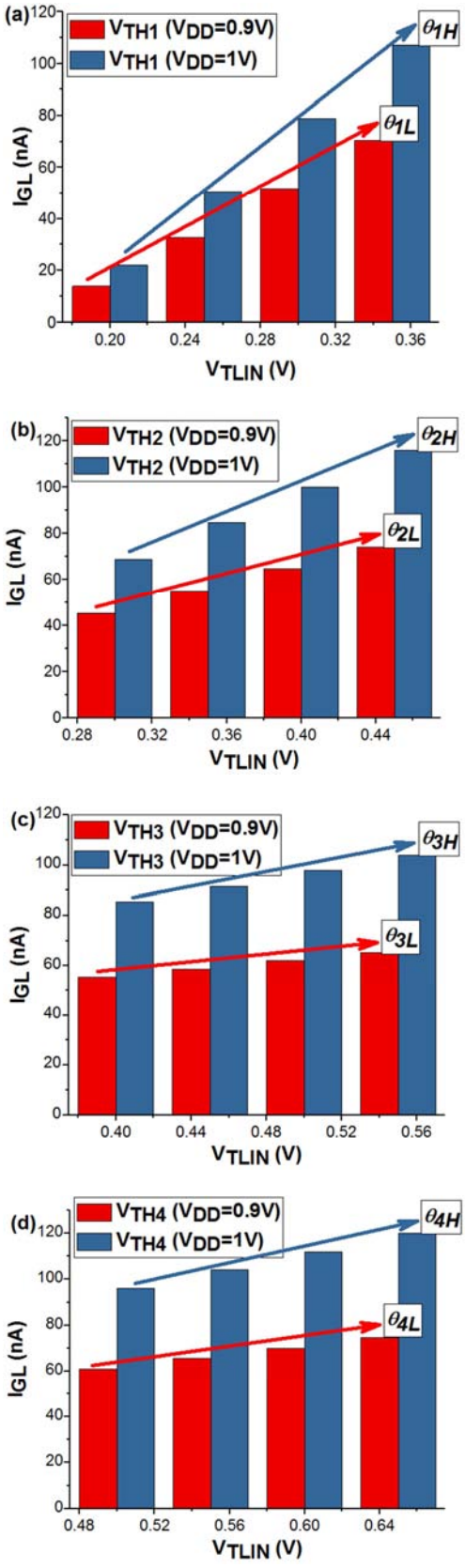


Figure 6. *The rate of accretion of the gate leakage current vs. threshold voltage curve escalates with the increase in the power supply voltage (a)-(d) The plots illustrate that when V_{DD} increases from 0.9V to 1V, the slope of (I_{GL})-(V_{TLIN}) plot increases for all four types of considered device designs.*

Table 3. *Rate of Accretion of Gate Leakage Current vs. Threshold Voltage.*

Parameter	Θ_L (V_{DD}=0.9V)	Θ_H (V_{DD}=1V)
V_{TH1}	3.78e-7	5.68e-7
V_{TH2}	1.91e-7	3.18e-7
V_{TH3}	6.53e-8	1.24e-7
V_{TH4}	9.14e-8	1.61e-7

The rate of accretion of the gate leakage current vs. threshold voltage curve escalates with the increase in the power supply voltage. Figure. 6(a)-(d) additionally demonstrates the (I_{GL})-(V_{TLIN}) plot slope, $S_{GL}=d\ (I_G)/d(V_{TLIN})$ increments with the supply voltage for all the device design lot ($V_{TH1} - V_{TH4}$), which is in concurrence with the proffered model (4) and (7). It presents the comparative TCAD simulation results of the gate leakage slope for V_{DD} = 0.9V and V_{DD} = 1V in the bar graph format. The rate of accretion of log (I_{GL}) vs. V_{TH} variations for discrete design lot (V_{TH1} *to* V_{TH4}) is respectively represented by Θ_1 to Θ_4. The added subscript L/H corresponds to low/high power supply i.e. V_{DD}=0.9V/1V. For precise and specific results, Table III represents the simulation outcomes in tabular format. It is clearly observed that the slope of (I_{GL})-(V_{TLIN}) plot increases for all four types of device designs.

5. Conclusion

The manuscript exhibited and proffered a physical model on the inconsistent relationship between the gate leakage current and threshold voltage variance precisely for nano scaled MOSFETs. The study and analysis presented in the manuscript has not been presently implemented in conventional gate leakage device models. The experimental results and the outcomes cannot be clarified by previously presented gate leakage models which attribute the evident threshold voltage variance to gate leakage current flowing through the gate resistance. Rather, the manuscript explores that the threshold voltage and gate leakage current (V_{TH})-(I_{GL}) characteristics can be precisely clarified and justified by short-channel impacts, in particular, the threshold voltage roll-off impact, along with a surface potential dependent gate leakage model. The tunneling gate leakage current density (J_{GL}) diminishes with V_{TH} over surface potential (ψ_s). However, the threshold voltage roll-off impact causes higher V_{TH} for larger channel length (L_G) devices. The net gate leakage current is adjusted by these two contrary functions of threshold voltage. In addition, the rate of accretion of the gate leakage current with threshold voltage variation is also analyzed. The impact of the increase in the power supply voltage on the rate of accretion of the gate leakage current vs. threshold voltage curve is also explored. Thorough methodical TCAD simulations were accomplished to validate the proffered models. Both the experimental outcomes, TCAD simulations and physics based models were implemented to uncover and clarify the Threshold voltage and gate leakage relationship, particularly for nano MOSFETs. The future nano device models ought to envelop these inconsistent (V_{TH})-(I_{GL}) characteristics enlightened in this comprehensive study to enhance the precision of gate leakage current in power proficient, multi-threshold voltage circuit design and reliability analysis.

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Biography

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